

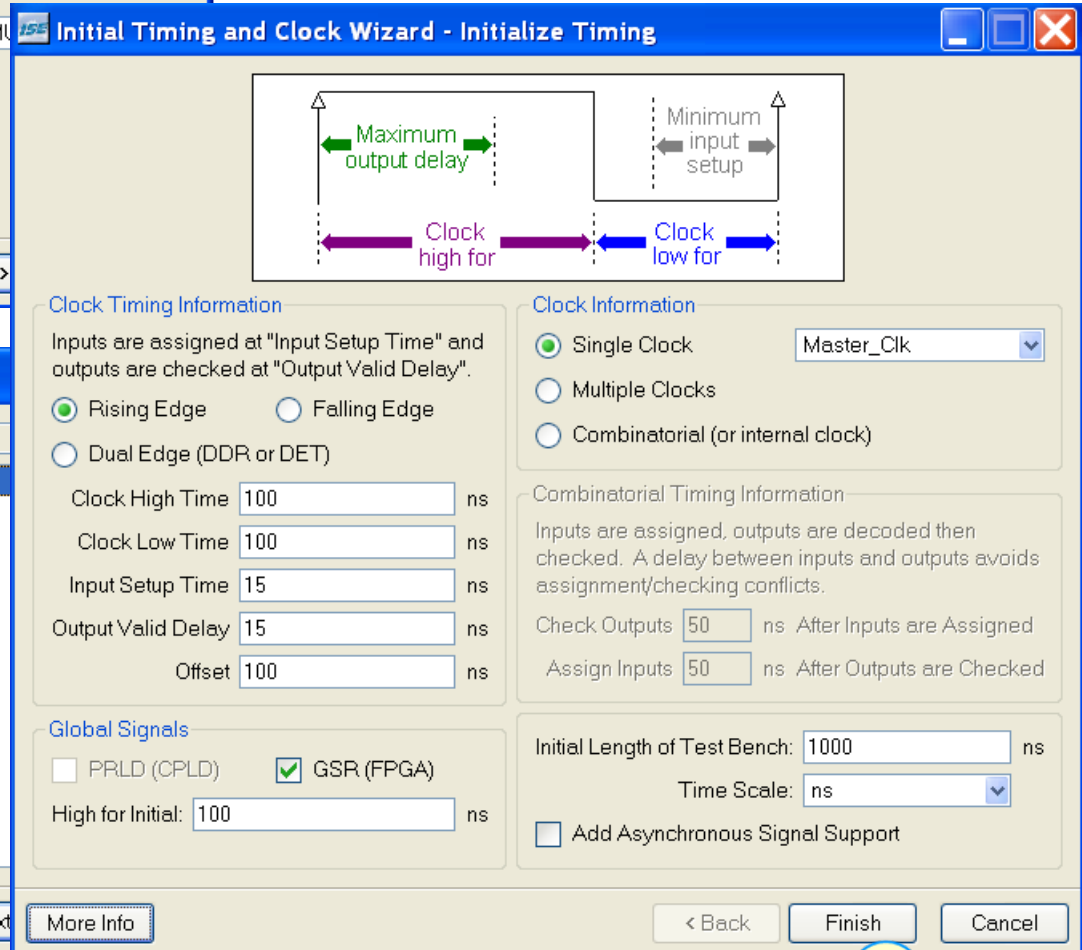
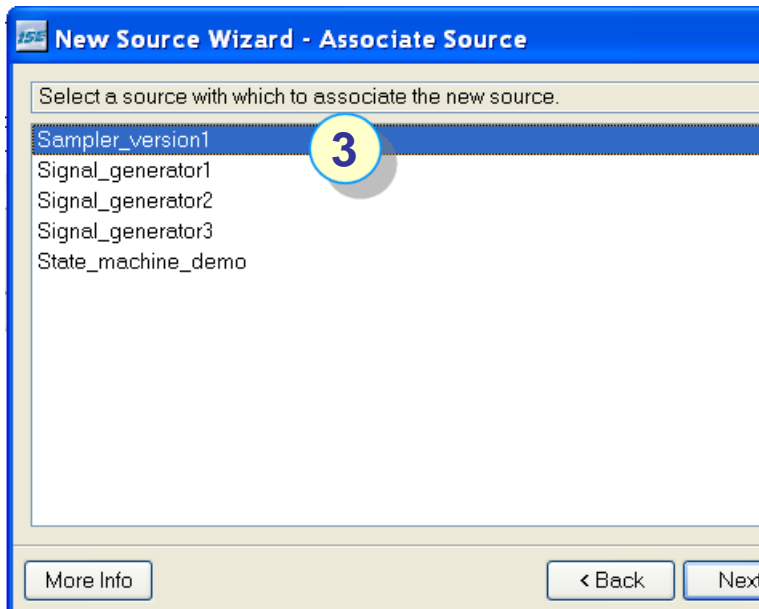
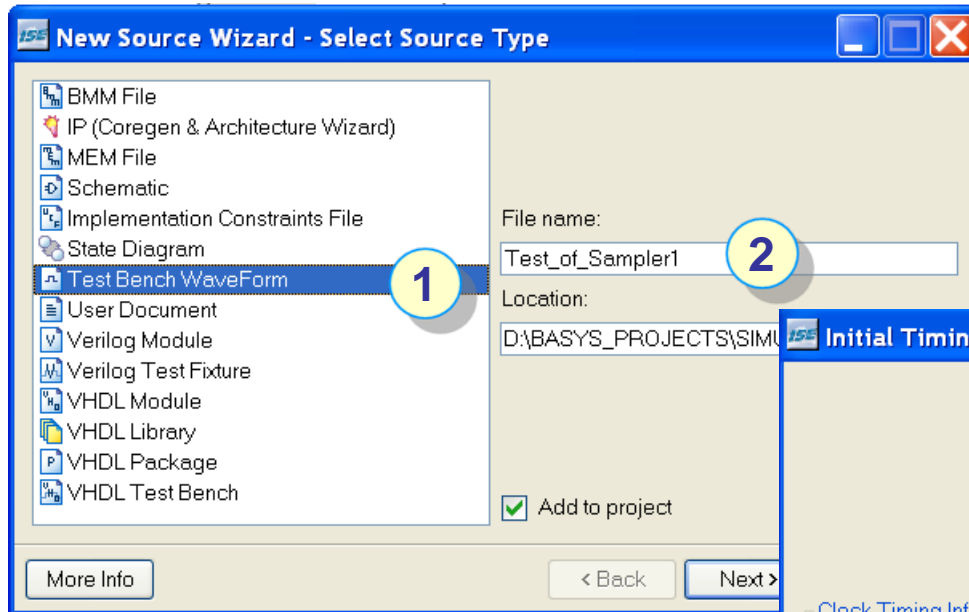
VHDL for simulation – Code for synthesizable

```
8 entity Sampler_version1 is
9   Port ( Master_Clk : in  STD_LOGIC;
10         Datin  :      in  STD_LOGIC_VECTOR (7 downto 0);
11         Datout :      out STD_LOGIC_VECTOR (7 downto 0);
12         Clks   :      out STD_LOGIC);
13 end Sampler_version1;
14
15 architecture Behavioral of Sampler_version1 is
16   signal Q: STD_LOGIC_VECTOR (7 downto 0);
17   signal Enb: STD_LOGIC;
18 begin
19
20   Clks  <= not Enb;
21   Datout <= not Q;  -- Alternative Q+1
22
23   process ( Master_Clk)
24     variable Scale: integer range 0 to 3 := 1;
25   begin
26     if rising_edge ( Master_Clk) then
27       if Scale > 0 then
28         Scale := Scale-1;
29         Enb  <= '0';
30       else
31         Scale := 2;
32         Enb  <= '1';
33       end if;
34     end if;
35   end process;
36
37   process ( Master_Clk)
38   begin
39     if rising_edge ( Master_Clk) then
40       if Enb='1' then
41         Q <= Datin;
42       end if;
43     end if;
44   end process;
45
46 end Behavioral;
```



```
4  -- Notes:
5  -- 1) This instantiation template has been automatically generated using types
6  -- std_logic and std_logic_vector for the ports of the instantiated module
7  -- 2) To use this template to instantiate this entity, cut-and-paste and then edit
8
9  COMPONENT Sampler_version1
10 PORT(
11   Master_Clk : IN std_logic;
12   Datin : IN std_logic_vector(7 downto 0);
13   Datout : OUT std_logic_vector(7 downto 0);
14   Clks : OUT std_logic
15 );
16 END COMPONENT;
17
18 Inst_Sampler_version1: Sampler_version1 PORT MAP (
19   Master_Clk => ,
20   Datin => ,
21   Datout => ,
22   Clks =>
23 );
```

The TestBenchWaveForm – Tool (1)



The TestBenchWaveForm – Tool (2)

The screenshot displays the Xilinx ISE environment. The main window shows a waveform editor for a testbench named 'Test_of_Sampler1.tbw*'. The waveform is set to a duration of 1000 ns. A 'Set Value' dialog box is open, prompting the user to enter a hexadecimal value. The value '55' is entered in the text field. The dialog box has 'OK', 'Cancel', and 'Help' buttons. The waveform shows signals for 'Master_Clk', 'Datin[7:0]', 'Clks', and 'Datout[7:0]'. The 'Datin[7:0]' signal is shown with a value of 8'h00 from 0 to 400 ns, and 8'h55 from 400 to 1000 ns. The 'Datout[7:0]' signal is shown with a value of 8'h00 from 0 to 1000 ns. The 'Set Value' dialog box is annotated with a circled '2' next to the input field and a circled '3' next to the 'OK' button. A circled '1' is also present in the waveform editor area.

End Time: 1000 ns

1

2

3

Set Value

Enter the desired hexadecimal value:

55

Pattern Wizard

OK Cancel Help

Compiling vhdl file "D:/BASYS_PROJECTS/SIMULATION/Demo1/Demo1/Sampler_version1.vhd" in Library work.
Entity <sampler_version1> compiled.
Entity <sampler_version1> (Architecture <behavioral>) compiled.

Ready

Time: 221.3 ns

Behavioral Simulation (1)

The screenshot shows the Xilinx ISE IDE interface. The title bar indicates the project is 'D:\BASYS_PROJECTS\SIMULATION\Demo1\Demo1.ise' with a VHDL file named '[Sampler_version1.vhd]'. The menu bar includes File, Edit, View, Project, Source, Process, Window, and Help. The toolbar contains various icons for file operations and simulation. The 'Sources for: Behavioral Simulation' pane on the left shows a project tree with 'Demo1' containing 'xc3s100e-4tq144' and several behavioral sources. 'Test_of_Sampler1 (Test_of_Sampler1.tbw)' is highlighted with a red circle labeled '1'. Below it, the 'Processes for: Test_of_Sampler1' pane shows options like 'Add Existing Source', 'Create New Source', 'View Generated Test Bench As HDL', 'Add Test Bench To Project', 'Xilinx ISE Simulator', and 'Simulate Behavioral Model', which is highlighted with a red circle labeled '2'. The main editor window shows the following VHDL code:

```
22
23
24     process( Master_Clk)
25         variable Scale: integer range 0 to 3 := 1;
26     begin
27         if rising_edge( Master_Clk) then
28             if Scale > 0 then
29                 Scale := Scale-1;
30                 Enb    <= '0';
31             else
32                 Scale := 2;
33                 Enb    <= '1';
34             end if;
35         end if;
36     end process;
37
38     process( Master_Clk)
39     begin
40         if rising_edge( Master_Clk) then
41             if Enb='1' then
42                 Q <= Datin;
43             end if;
44         end if;
45     end process;
46 end Behavioral;
47
48
```

The status bar at the bottom shows 'Ready' on the left and 'Ln 42 Col 17 | CAPS NUM SCRL VHDL' on the right. The bottom pane shows tabs for 'Design Summary', 'State_machine_demo.vhd', and 'Sampler_version1.vhd'.

Behavioral Simulation (2)

The screenshot displays the Xilinx ISE Behavioral Simulation interface. The window title is "Xilinx - ISE - D:\BASYS_PROJECTS\SIMULATION\Demo1\Demo1.ise - [Simulation]". The menu bar includes File, Edit, View, Project, Source, Process, TestBench, Simulation, Window, and Help. The toolbar contains various simulation and editing tools, with a dropdown menu set to "number_data" and a time scale of "1000 ns".

The left pane shows the "Sources for: Behavioral Simulation" tree, listing files under "Demo1":

- xc3s100e-4tq144
 - Signal_generator1 - Behavioral (Signal_generator1.vhd)
 - Signal_generator2 - Behavioral (Signal_generator2.vhd)
 - Signal_generator3 - Behavioral (Signal_generator3.vhd)
 - State_machine_demo - Behavioral (State_machine_demo.v)
 - Test_of_Sampler1 (Test_of_Sampler1.tbw)

The bottom-left pane shows the "Test_of_Sampler1 - Test_of_Sampler1" hierarchy:

- Datout [7:0]
- Clks
- Datin [7:0]
- Master_Clk
- PERIOD [31:0]
- DUTY_CYCLE
- OFFSET [31:0]
- UUT - Sampler_version1 - Behavioral

The main window displays a timing diagram for "Current Simulation Time: 1000 ns". The time axis ranges from 0 to 1000 ns. The diagram shows the following signals:

- Datout[7:0]**: 8-bit output bus. It is initially 8'hXX (unknown) and transitions to 8'h56 at approximately 600 ns.
- Datout[7]**: 0
- Datout[6]**: 1
- Datout[5]**: 0
- Datout[4]**: 1
- Datout[3]**: 0
- Datout[2]**: 1
- Datout[1]**: 1
- Datout[0]**: 0
- Clks**: 0
- Datin[7:0]**: 8-bit input bus. It is initially 8'h00 and transitions to 8'h55 at approximately 600 ns.
- Master_Clk**: 1

The bottom status bar shows "Time: ---" and the active window is "Simulation".

Behavioral Simulation (3)

The screenshot displays the Xilinx ISE Behavioral Simulation environment. The main window shows a waveform for a simulation of a divider circuit. The waveform has a time axis from 0 to 1000 ns. A signal labeled 'number_data' is shown at the top right with a value of 950.0. The waveform shows several signals, including '8'h00' and '8'h55', and a signal labeled 'enb' which is a pulse. A 'Divider' dialog box is open, showing the configuration for a divider with the label 'Divider with text'. The dialog has fields for 'Divider Label', 'Divider Height', 'Background Color', and 'Label Text Color'. The 'Background Color' is set to 'Dark grey' and 'Label Text Color' is set to 'White'. A 'Rightclick' context menu is also visible, showing options like 'Reverse Bus', 'Delete', 'Decimal (Signed)', 'Decimal (Unsigned)', 'Hexadecimal', 'Binary', 'ASCII', 'Find Signal...', 'Sort Signals Ascending', 'Sort Signals Descending', 'Add Divider...', and 'Show Driver...'. A 'Drag and drop' callout points to the 'enb' signal in the waveform. A 'Simulation' menu is open, showing options like 'Restart', 'Stop', 'Step', 'Run All', 'Run For Specified Time', 'Goto Previous Transition', 'Goto Next Transition', 'Goto Time...', 'Goto Marker', 'Find Signal...', 'Sort Signals Ascending', 'Sort Signals Descending', 'Markers', 'Zoom', and 'End Simulation'.

Simulation Menu:

- Restart
- Stop
- Step
- Run All
- Run For Specified Time
- Goto Previous Transition
- Goto Next Transition
- Goto Time...
- Goto Marker
- Find Signal...
- Sort Signals Ascending
- Sort Signals Descending
- Markers
- Zoom
- End Simulation

Divider Dialog:

- Divider Label: Divider with text
- Divider Height: 20
- Background Color: Dark grey
- Label Text Color: White
- Note: If the Divider Height is made too small the label may not appear.
- Buttons: OK, Cancel, Help

Rightclick Context Menu:

- Reverse Bus
- Delete
- Decimal (Signed)
- Decimal (Unsigned)
- Hexadecimal
- Binary
- ASCII
- Find Signal...
- Sort Signals Ascending
- Sort Signals Descending
- Add Divider...
- Show Driver...

Callouts:

- Drag and drop
- Rightclick

Behavioral Simulation (4)

Restart the simulation

Run for 1000 ns

Simulation menu options:

- Restart
- Stop
- Step
- Run All
- Run For Specified Time
- Goto Previous Transition
- Goto Next Transition
- Goto Time...
- Goto Marker
- Find Signal...
- Sort Signals Ascending
- Sort Signals Descending
- Markers
- Zoom
- End Simulation

Timing diagram signals:

- number_data: 8'h00, 8'h56, 8'h55
- enb: 0
- Master_Clk: 1
- Divider with text

Context menu options:

- Zoom In
- Zoom Out
- Zoom Full View
- Add Measure
- Add Marker
- Grid
- Goto Time...
- Goto Marker

Adding the TestBench to the Project

The screenshot displays the Xilinx ISE interface during a simulation. The main window shows a waveform for 'Current Simulation Time: 2000 ns'. The waveform includes signals such as Datout[7:0], Clks, Datin[7:0], Master_Clk, enb, and q[7:0]. A vertical blue line indicates the current simulation time at 950.0 ns. The waveform shows Datout[7:0] changing from 8'hXX to 8'hAA, Datin[7:0] changing from 8'h00 to 8'h55, and q[7:0] changing from 8'hUU to 8'h55. The 'Processes for: Test_of_Sampler1' window is open, showing the 'Add Test Bench To Project' option selected. The 'Sources for: Behavioral Simulation' window shows the 'Test_of_Sampler1.tbw' file selected.

1

2

Time: 1934.2 ns

Changing Preferred Language to VHDL

Sources for: Behavioral Simulation

- xc3s100e-4tq144
- Signal_generator1 - Behavioral (Signal_generator1.vhd)
- Signal_generator2 - Behavioral (Signal_generator2.vhd)
- Signal_generator3 - Behavioral (Signal_generator3.vhd)
- State_machine_demo - Behavioral (State_machine_demo.vhd)
- Test_of_Sampler1 (Test_of_Sampler1.tbw)
- UUT - Sampler_version1 - Behavioral (Sampler_version1.vhd)
- Test_of_Sampler1_tb_0 (Test_of_Sampler1_tb_0.v)**
- UUT - Sampler_version1 - Behavioral (Sampler_version1.vhd)

```
parameter PERIOD = 200;
parameter real DUTY_CYCLE = 0.5;
parameter OFFSET = 100;

initial // Clock process for Master_Clk
begin
  #OFFSET;
  forever
  begin
    Master_Clk = 1'b0;
    #(PERIOD-(PERIOD*DUTY_CYCLE)) Master_Clk = 1'b1;
    #(PERIOD*DUTY_CYCLE);
  end
end

Sampler_version1 UUT (
  .Master_Clk (Master_Clk) ,
  .Datin (Datin) ,
  .Datout (Datout) ,
  .Clks (Clks) );

initial begin
  // ----- Current Time: 185ns
  #185;
  Datin = 8'b01010101;
  // -----
end

endmodule
```

Property Name	Value
Product Category	All
Family	Spartan3E
Device	XC3S100E
Package	TQ144
Speed	-4
Top-Level Source Type	HDL
Synthesis Tool	XST (VHDL/Verilog)
Simulator	ISE Simulator (VHDL/Verilog)
Preferred Language	VHDL
Enable Enhanced Design Summary	Verilog
Enable Message Filtering	<input type="checkbox"/>

OK Cancel Default Help

Summary State_machine_dem Sampler_version Simulation Test_of_Sampler1_t

Ln 1 Col 1 CAPS NUM SCRL Verilog

Sources for: Behavioral Simulation

- Demot
 - xc3s100e-4tq144
 - Signal_generator1 - Behavioral (Signal_generator1.vhd)
 - Signal_generator2 - Behavioral (Signal_generator2.vhd)
 - Signal_generator3 - Behavioral (Signal_generator3.vhd)
 - State_machine_demo - Behavioral (State_machine_demo.vhd)
 - Test_of_Sampler1_tb_0 - testbench_arch (Test_of_Sampler1_tb_0.vhd)** 6
 - UUT - Sampler_version1 - Behavioral (Sampler_version1.vhd)
 - Test_of_Sampler1 (Test_of_Sampler1.tbw)
 - UUT - Sampler_version1 - Behavioral (Sampler_version1.vhd)
 - Test_of_Sampler1_tb_0 (Test_of_Sampler1_tb_0.v)
 - UUT - Sampler_version1 - Behavioral (Sampler_version1.vhd)

Sources Snapshots Libraries

Processes for: Test_of_Sampler1_tb_0 - testbench

- Add Existing Source
- Create New Source
- Xilinx ISE Simulator
 - Check Syntax
 - Simulate Behavioral Model

Processes Sim Hierarchy - Test_of_Sampler1

```

44 SIGNAL Datout : std_logic_vector (7 DownTo 0) := "000001";
45 SIGNAL Clks : std_logic := '0';
46
47 constant PERIOD : time := 200 ns;
48 constant DUTY_CYCLE : real := 0.5;
49 constant OFFSET : time := 100 ns;
50 BEGIN
51 UUT : Sampler_version1
52 PORT MAP ( Master_Clk => Master_Clk,
53           Datin => Datin,
54           Datout => Datout,
55           Clks => Clks);
56
57 PROCESS -- clock process for Master_Clk
58 BEGIN
59 WAIT for OFFSET;
60 CLOCK_LOOP : LOOP
61 Master_Clk <= '0';
62 WAIT FOR (PERIOD - (PERIOD * DUTY_CYCLE));
63 Master_Clk <= '1';
64 WAIT FOR (PERIOD * DUTY_CYCLE);
65 END LOOP CLOCK_LOOP;
66 END PROCESS;
67
68 PROCESS
69 BEGIN
70 ----- Current Time: 185ns
71 WAIT FOR 185 ns;
72 Datin <= "01010101";
73 -----
74 WAIT FOR 1015 ns;
75 END PROCESS;
76 END testbench_arch;

```

Generate Self-Checking TestBench

Sources for: Behavioral Simulation

- Demo1
 - xc3s100e-4tq144
 - Signal_generator1 - Behavioral (Signal_generator1.vhd)
 - Signal_generator2 - Behavioral (Signal_generator2.vhd)
 - Signal_generator3 - Behavioral (Signal_generator3.vhd)
 - State_machine_demo - Behavioral (State_machine_demo.vhd)
 - Test_of_Sampler1_selfcheck_beh - testbench_arch (Test_of_Sampler1_selfcheck_beh.vhd)
 - UUT - Sampler_version1 - Behavioral (Sampler_version1.vhd)
 - Test_of_Sampler1_tb_0 - testbench_arch (Test_of_Sampler1_tb_0.vhd)
 - Test_of_Sampler1 (Test_of_Sampler1.tbw)
 - Test_of_Sampler1_tb_0 (Test_of_Sampler1_tb_0.v)
 - UUT - Sampler_version1 - Behavioral (Sampler_version1.vhd)

Processes for: Test_of_Sampler1

- Add Existing Source
- Create New Source
- View Generated Test Bench As HDL
- Add Test Bench To Project
- Xilinx ISE Simulator
 - Simulate Behavioral Model
 - Generate Self-Checking Test Bench

```
1  -----
2  -- Copyright (c) 1995-2007 Xilinx, Inc.
3  -- All Right Reserved.
4  -----
5  --
6  --
7  -- Vendor: Xilinx
8  -- Version : 9.2.04i
9  -- Application : ISE
10 -- Filename : Test_of_Sampler1_selfcheck.vh
11 -- Timestamp : Sun Feb 10 10:23:47 2008
12 --
13 --
14 --
15 --Command:
16 --Design Name: Test_of_Sampler1_selfcheck_beh
17 --Device: Xilinx
18 --
19
20 library IEEE;
21 use IEEE.STD_LOGIC_1164.ALL;
22 use IEEE.STD_LOGIC_ARITH.ALL;
23 use IEEE.STD_LOGIC_UNSIGNED.ALL;
24 USE IEEE.STD_LOGIC_TEXTIO.ALL;
25 USE STD.TEXTIO.ALL;
26
27 ENTITY Test_of_Sampler1_selfcheck_beh IS
28 END Test_of_Sampler1_selfcheck_beh;
29
30 ARCHITECTURE testbench_arch OF Test_of_Sampler1_selfcheck
31 COMPONENT Sampler_version1
32 PORT (
33     Master Clk : In std logic;
```

Design Summary | State_machine | Sampler_version1 | Test_of_Sample | Test_of_Sampler1_self

Ln 1 Col 1 | CAPS | NUM | SCRL | VHDL

Selfchecking TestBench (1)

```
20 library IEEE;
21 use IEEE.STD_LOGIC_1164.ALL;
22 use IEEE.STD_LOGIC_ARITH.ALL;
23 use IEEE.STD_LOGIC_UNSIGNED.ALL;
24 USE IEEE.STD_LOGIC_TEXTIO.ALL;
25 USE STD.TEXTIO.ALL;
26
27 ENTITY Test_of_Sampler1_selfcheck_beh IS
28 END Test_of_Sampler1_selfcheck_beh;
29
30 ARCHITECTURE testbench_arch OF Test_of_Sampler1_selfcheck_beh IS
31     COMPONENT Sampler_version1
32     PORT (
33         Master_Clk : In std_logic;
34         Datin : In std_logic_vector (7 DownTo 0);
35         Datout : Out std_logic_vector (7 DownTo 0);
36         Clks : Out std_logic
37     );
38 END COMPONENT;
39
40 SIGNAL Master_Clk : std_logic := '0';
41 SIGNAL Datin : std_logic_vector (7 DownTo 0) := "00000000";
42 SIGNAL Datout : std_logic_vector (7 DownTo 0) := "UUUUUUUUU";
43 SIGNAL Clks : std_logic := 'U';
44
45 SHARED VARIABLE TX_ERROR : INTEGER := 0;
46 SHARED VARIABLE TX_OUT : LINE;
47
48 constant PERIOD : time := 200 ns;
49 constant DUTY_CYCLE : real := 0.5;
50 constant OFFSET : time := 100 ns;
51
52 BEGIN
53     UUT : Sampler_version1
54     PORT MAP (
55         Master_Clk => Master_Clk,
56         Datin => Datin,
57         Datout => Datout,
58         Clks => Clks
59     );
```


Selfchecking TestBench (2)

```
60
61 PROCESS    -- clock process for Master_Clk
62 BEGIN
63     WAIT for OFFSET;
64     CLOCK_LOOP : LOOP
65         Master_Clk <= '0';
66         WAIT FOR (PERIOD - (PERIOD * DUTY_CYCLE));
67         Master_Clk <= '1';
68         WAIT FOR (PERIOD * DUTY_CYCLE);
69     END LOOP CLOCK_LOOP;
70 END PROCESS;
71
72 PROCESS
73     PROCEDURE CHECK_Clks (
74         next_Clks : std_logic;
75         TX_TIME : INTEGER
76     ) IS
77         VARIABLE TX_STR : String(1 to 4096);
78         VARIABLE TX_LOC : LINE;
79         BEGIN
80             IF (Clks /= next_Clks) THEN
81                 STD.TEXTIO.write(TX_LOC, string("Error at time="));
82                 STD.TEXTIO.write(TX_LOC, TX_TIME);
83                 STD.TEXTIO.write(TX_LOC, string("ns Clks="));
84                 IEEE.STD_LOGIC_TEXTIO.write(TX_LOC, Clks);
85                 STD.TEXTIO.write(TX_LOC, string(", Expected = "));
86                 IEEE.STD_LOGIC_TEXTIO.write(TX_LOC, next_Clks);
87                 STD.TEXTIO.write(TX_LOC, string(" "));
88                 TX_STR(TX_LOC.all'range) := TX_LOC.all;
89                 STD.TEXTIO.Deallocate(TX_LOC);
90                 ASSERT (FALSE) REPORT TX_STR SEVERITY ERROR;
91                 TX_ERROR := TX_ERROR + 1;
92             END IF;
93         END;
```

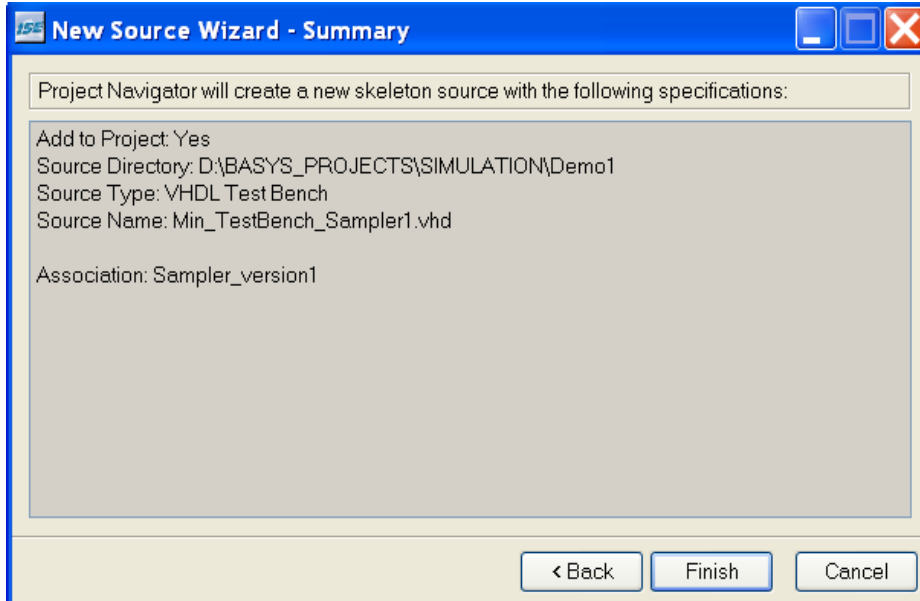
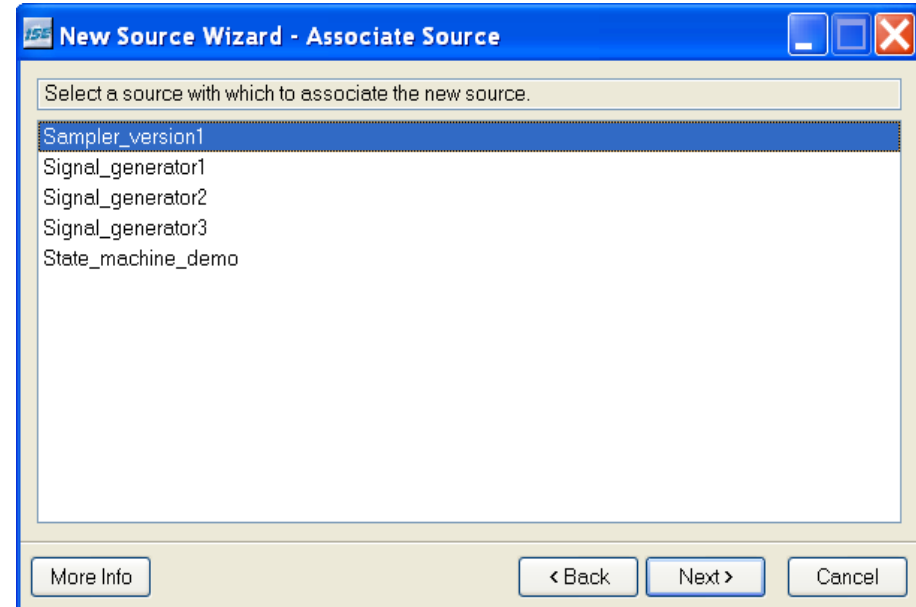
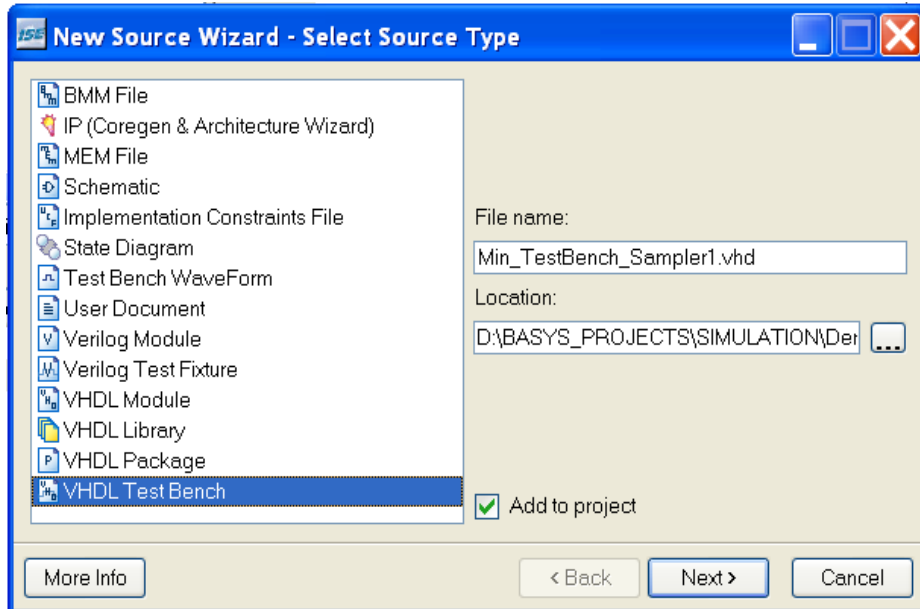

Selfchecking TestBench (3)

```
94  PROCEDURE CHECK_Datout(  
95      next_Datout : std_logic_vector (7 DownTo 0);  
96      TX_TIME : INTEGER  
97  ) IS  
98      VARIABLE TX_STR : String(1 to 4096);  
99      VARIABLE TX_LOC : LINE;  
100     BEGIN  
101     IF (Datout /= next_Datout) THEN  
102         STD.TEXTIO.write(TX_LOC, string("Error at time="));  
103         STD.TEXTIO.write(TX_LOC, TX_TIME);  
104         STD.TEXTIO.write(TX_LOC, string("ns Datout="));  
105         IEEE.STD_LOGIC_TEXTIO.write(TX_LOC, Datout);  
106         STD.TEXTIO.write(TX_LOC, string(", Expected = "));  
107         IEEE.STD_LOGIC_TEXTIO.write(TX_LOC, next_Datout);  
108         STD.TEXTIO.write(TX_LOC, string(" "));  
109         TX_STR(TX_LOC.all'range) := TX_LOC.all;  
110         STD.TEXTIO.Deallocate(TX_LOC);  
111         ASSERT (FALSE) REPORT TX_STR SEVERITY ERROR;  
112         TX_ERROR := TX_ERROR + 1;  
113     END IF;  
114 END;  
115 BEGIN  
116     -- ----- Current Time: 185ns  
117     WAIT FOR 185 ns;  
118     Datin <= "01010101";  
119     -----  
120     -- ----- Current Time: 215ns  
121     WAIT FOR 30 ns;  
122     CHECK_Clks('1', 215);  
123     -----  
124     -- ----- Current Time: 415ns  
125     WAIT FOR 200 ns;  
126     CHECK_Clks('0', 415);  
127     -----  
128     -- ----- Current Time: 615ns  
129     WAIT FOR 200 ns;  
130     CHECK_Clks('1', 615);  
131     CHECK_Datout("10101010", 615);  
132     -----  
133     WAIT FOR 585 ns;
```

Selfchecking TestBench (4)

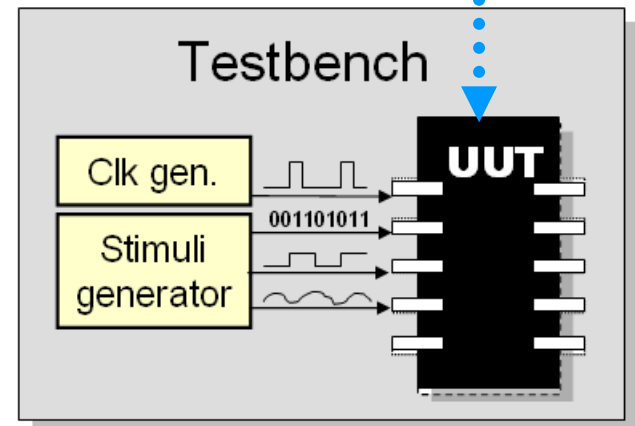
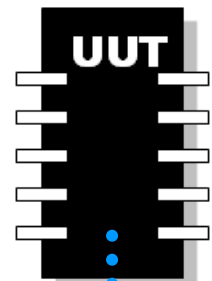
```
134
135     IF (TX_ERROR = 0) THEN
136         STD.TEXTIO.write(TX_OUT, string("No errors or warnings"));
137         ASSERT (FALSE) REPORT
138             "Simulation successful (not a failure). No problems detected."
139             SEVERITY FAILURE;
140     ELSE
141         STD.TEXTIO.write(TX_OUT, TX_ERROR);
142         STD.TEXTIO.write(TX_OUT,
143             string(" errors found in simulation"));
144         ASSERT (FALSE) REPORT "Errors found during simulation"
145             SEVERITY FAILURE;
146     END IF;
147 END PROCESS;
148
149 END testbench_arch;
```

Creating your own TestBench (1)



Creating your own TestBench (2)

```
23 -- This testbench has been automatically generated using types std_logic and
24 -- std_logic_vector for the ports of the unit under test.  Xilinx recommends
25 -- that these types always be used for the top-level I/O of a design in order
26 -- to guarantee that the testbench will bind correctly to the post-implementation
27 -- simulation model.
28 -----
29 LIBRARY ieee;
30 USE ieee.std_logic_1164.ALL;
31 USE ieee.std_logic_unsigned.all;
32 USE ieee.numeric_std.ALL;
33
34 ENTITY Min_TestBench_Sampler1_vhd IS
35 END Min_TestBench_Sampler1_vhd;
36
37 ARCHITECTURE behavior OF Min_TestBench_Sampler1_vhd IS
38 ----- Component Declaration for the Unit Under Test (UUT)
39 COMPONENT Sampler_version1
40 PORT(
41     Master_Clk : IN  std_logic;
42     Datin      : IN  std_logic_vector(7 downto 0);
43     Datout     : OUT std_logic_vector(7 downto 0);
44     Clks       : OUT std_logic);
45 END COMPONENT;
46 ----- Inputs
47 SIGNAL Master_Clk : std_logic := '0';
48 SIGNAL Datin      : std_logic_vector(7 downto 0) := (others=>'0');
49 ----- Outputs
50 SIGNAL Datout     : std_logic_vector(7 downto 0);
51 SIGNAL Clks       : std_logic;
52 BEGIN
53 ----- Instantiate the Unit Under Test
54 UUT: Sampler_version1 PORT MAP ( Master_Clk => Master_Clk,
55                                 Datin      => Datin,
56                                 Datout     => Datout,
57                                 Clks       => Clks );
58
59 tb : PROCESS
60 BEGIN
61     -- Wait 100 ns for global reset to finish
62     wait for 100 ns;
63     -- Place stimulus here
64     wait; -- will wait forever
65 END PROCESS;
66 END;
```



File Edit View Project Source Process TestBench Simulation Window Help

number_data 2000 ns

Sources for: Behavioral Simulation

- Demo1
 - xc3s100e-4tq144
 - Min_TestBench_Sampler1_vhd - behavior (Min_TestBench_Sample...
 - Signal_generator1 - Behavioral (Signal_generator1.vhd)
 - Signal_generator2 - Behavioral (Signal_generator2.vhd)

Testbench

- clks
- clk_v1
- delta_step
- delta
- delta_xx
- UUT - Sampler_version1 - Behavioral
 - master_clk
 - datin [7:0]
 - datout [7:0]
 - clks
 - q [7:0]
 - enb

Current Simulation Time: 2000 ns

950.0

Signal	Value	0	400	800	1200	1600	2000
clkx	1	High	High	High	High	High	High
dataout[7:0]	8...	00110101	00110101	00110101	00110101	00110101	00110101
master_clk	0	High	High	High	High	High	High
clks	0	High	High	High	High	High	High
datin[7:0]	8...	00110101	00110101	00110101	00110101	00110101	00110101
datin[7]	0	0	0	0	0	0	0
datin[6]	1	1	1	1	1	1	1
datin[5]	0	0	0	0	0	0	0
datin[4]	1	1	1	1	1	1	1
datin[3]	1	1	1	1	1	1	1
datin[2]	0	0	0	0	0	0	0
datin[1]	1	1	1	1	1	1	1
datin[0]	1	1	1	1	1	1	1
q[7:0]	8...	00110101	00110101	00110101	00110101	00110101	00110101
q[7]	0	0	0	0	0	0	0
q[6]	1	1	1	1	1	1	1
q[5]	0	0	0	0	0	0	0
q[4]	1	1	1	1	1	1	1
q[3]	0	0	0	0	0	0	0
q[2]	1	1	1	1	1	1	1
q[1]	1	1	1	1	1	1	1
q[0]	0	0	0	0	0	0	0
datout[7:0]	8...	00110101	00110101	00110101	00110101	00110101	00110101
datout[7]	1	1	1	1	1	1	1
datout[6]	0	0	0	0	0	0	0
datout[5]	1	1	1	1	1	1	1
datout[4]	0	0	0	0	0	0	0
datout[3]	1	1	1	1	1	1	1
datout[2]	0	0	0	0	0	0	0
datout[1]	0	0	0	0	0	0	0
datout[0]	1	1	1	1	1	1	1

Processes: Sim Hierarchy - Min_TestBench_Sampler1_vhd

Design Summary | Min_TestBench_Sampler1.vhd | Simulation

Modelsim able to present signals as Analog

The screenshot shows the Modelsim interface with a waveform viewer. The left pane shows a tree view of signals, including `/min_testbench_sampl1_vhd/clkx`, `/min_testbench_sampl1_vhd/dataout`, `/min_testbench_sampl1_vhd/master_clk`, `/min_testbench_sampl1_vhd/datin`, `/min_testbench_sampl1_vhd/datout`, `/min_testbench_sampl1_vhd/clks`, and `/min_testbench_sampl1_vhd/clk_v1`. The waveform viewer displays a digital signal with a smooth analog curve overlaid. A yellow cursor is positioned at 61410 ps. The time scale is 100 ps. The signal is inverted for better presentation.

Wave Analog dialog box options:

- Format:
 - Analog Step
 - Analog Interpolated
 - Analog Backstep
- Pixels = (value + 500.0) * -0.5

Buttons: OK, Cancel, Apply

Note – This signal
been inverted for
a better presentation

Creating your own TestBench (3)

```
29 LIBRARY ieee;
30 USE ieee.std_logic_1164.ALL;
31 USE ieee.std_logic_unsigned.all;
32 USE ieee.numeric_std.ALL;
33 use IEEE.STD_LOGIC_ARITH.ALL;
34 use IEEE.MATH_REAL.ALL;           -- This contains the SIN( )
35
36 ENTITY Min_TestBench_Sampler1_vhd IS
37     Port ( CLKX:          out  STD_LOGIC;
38           Dataout :  inout  STD_LOGIC_VECTOR (7 downto 0));
39 END Min_TestBench_Sampler1_vhd;
40
41 ARCHITECTURE behavior OF Min_TestBench_Sampler1_vhd IS
42     ----- Component Declaration for the Unit Under Test (UUT)
43     COMPONENT Sampler_version1
44     PORT(   Master_Clk : IN  std_logic;
45           Datin  :    IN  std_logic_vector(7 downto 0);
46           Datout :    OUT std_logic_vector(7 downto 0);
47           Clks   :    OUT std_logic);
48     END COMPONENT;
49
50     ----- Inputs
51     SIGNAL Master_Clk : std_logic := '0';
52     SIGNAL Datin  :    std_logic_vector(7 downto 0) := (others=>'0');
53     ----- Outputs
54     SIGNAL Datout :    std_logic_vector(7 downto 0);
55     SIGNAL Clks   :    std_logic;
56
57     -----
58     signal Clk_v1:          STD_LOGIC := '0';
59     -- Please note - Shared variables can be used for interprocess data
60     -- exchange. Moreover can they be observed under a simulation as well
61     shared variable Delta_step: real := 100.0;
62     shared variable Delta:      real := 1000.0;
63     shared variable Delta_xx:   real := -1.0;
```

Creating your own TestBench (4)

```
63 BEGIN
64     ----- Instantiate the Unit Under Test (UUT)
65     UUT: Sampler_version1 PORT MAP ( Master_Clk => Master_Clk,
66                                     Datin      => Datin,
67                                     Datout     => Datout,
68                                     Clks       => Clks );
69
70     Master_Clk <= not Master_Clk after 5 ns;  -- 100 MHz master clock|
71     Datin      <= DataOut;
72     CLKX       <= Clk_v1;
73
74     -----
75     -- This process creates a clk-signal with a variable frequency
76     -- not use if its useful in practice, but it demonstrates what can
77     -- be done.
78     -- The shared variable "Delta" will decrease with the value "Delta_step"
79     -- for each step will the "Delta_step" value change with "Delta_xx"
80     -----
81     Clk_generator: process
82     begin
83         Clk_v1 <= not Clk_v1;  -- Toogle the Clk
84         Delta := 1000.0;      -- Ready for a new count down
85         while Delta>0.0 loop  -- while not done
86             wait for 10 ps;    -- adjust this if needed
87             Delta := Delta - Delta_step;  -- one step down
88         end loop;
89
90         if Delta_xx < 0.0 then
91             if Delta_step < 2.0 then
92                 Delta_xx := 0.1;
93             end if;
94         else
95             if Delta_step > 198.0 then
96                 Delta_xx := -0.1;
97             end if;
98         end if;
99         Delta_Step := Delta_step + Delta_xx;
100    end process Clk_generator;
```

Creating your own TestBench (5)

```
102 -----
103 -- This process driven by an external clock signal
104 -- the statement "wait until rising_edge( clk_v1)" do the trick
105 -----
106 Sinus_generator: process
107     constant Umax:      integer := 127;      -- Max amplitude
108     constant f:        real    := 2.0E6;    -- Frequency [Hz]
109     constant Tper:     real    := 1.0/f;    -- Period of fr.
110 -- If you can find a way to convert real to time please let me know
111     constant Delta:    real    := 1000.0E-12; -- delta time - sec
112     constant DeltaWait: time    := 1000 ps;  -- delta time - ps
113 -----
114     variable t:        Real := 0.0;  -- Actual time
115     variable angle:   real := 0.0;  -- Actual angle in radians
116     variable Usin:    real := 0.0;  -- The sin value [real]
117     variable Usin_int: integer;  -- The sin value as integer
118 begin
119     wait until rising_edge( Clk_v1);
120
121     angle := 2.0 * MATH_PI * t * f;  -- calculate angle
122     t := t + Delta;                  -- next time
123     Usin := real(Umax)*( SIN( angle)+1.0); -- Usin calculation
124     Usin_int := integer(Usin);      -- convert real to integer
125     Dataout <= conv_std_logic_vector( Usin_int, 8); -- to vector
126 end process sinus_generator;
127
128 ----- not in use -----
129 tb : PROCESS
130 BEGIN
131     -- Wait 100 ns for global reset to finish
132     wait for 100 ns;
133     -- Place stimulus here
134     wait; -- will wait forever
135 END PROCESS;
136 END;
```